REMARKS

Claims 1 to 6 and 10 to 13 were pending in the present application. Applicant has amended claims 1 and 11 to 13, and canceled claims 4 to 6.

Election/Restriction

Applicant affirms the election of the invention of Group I, claims 1 to 3 and 10 to 13 without traverse. Accordingly, Applicant cancels claims 4 to 6.

§ 103 Rejections of Claims 1 to 3, 10, and 12

The Examiner rejected claims 1 to 3, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,049,889 ("Steely, Jr. et al.") in view of U.S. Patent No. 5,850,556 ("Grivna").

Claim 1

Addressing claim 1, the Examiner found Applicant's previously submitted argument to be unpersuasive and restated his argument from the March 11, 2005 Office Action.

> In the description of col. 7, lines 13-32, Steely discloses an example of a write operation from a local node to a remote node (see col. 6, lines 47-50). Steely further teaches a direct memory access (DMA) command (col. 7, lines 29-30) for writing a block of data from a local node to a remote node (col. 7, lines 15-16) via the communication link (col. 9, lines 8-9).

September 12, 2005 Office Action. Applicant respectfully traverses.

Col. 7, lines 14 to 33 of Steely, Jr. et al. disclose a reflected write from a sender node 75 to a receiving node 85 shown in Fig. 7A. This reflected write is essentially the same as the reflected write shown in Fig. 5 except there are no address conversions from CPU to PCI memory space since memory channel (MC) adaptors 80 and 90 are located on system buses 78 and 88, respectively. The DMA operation cited by the Examiner at col. 7, lines 29 to 33, is a local operation performed by receiving node 85 to transfer the data received at its local MC adaptor to its local memory or local I/O device at the completion of the reflected write. In other words, the DMA operation transfers data from MC adaptor 90 to either a system memory 87 or a disk 92 in node 85. The DMA operation does not "writ[e] a block of data from a local node to a remote node via one of the communication links" as recited in amended claim 1. As the Examiner did not find Applicant's previous argument

persuasive, Applicant has submitted along with this Response a Rule 132 Declaration supporting Applicant's reading of Steely, Jr. et al.

Applicant has also amended claim 1 to recite "a memory copy write command for writing an entire line of memory from a local node to a remote node via one of the communication links when a new data is written into the line of memory even when the new data is smaller than the line of memory." Amended claim 1 (emphasis added). Thus, an entire line of memory is copied to a remote node for each memory copy write even when the new data is smaller than the line of memory. This saves overhead in the communication between nodes since the sending node does not need to specify the size of the data in memory copy writes. Steely Jr. et al. is silent as to this aspect of amended claim 1.

Accordingly, amended claim 1 is patentable over the combination of Steely Jr. et al. and Grivna for the above reasons.

Claims 2, 3, and 10

Claims 2, 3, and 10 depend from amended claim 1 and are patentable over the cited references for at least the same reasons as amended claim 1.

Claim 12

The Examiner rejected claim 12 in view of the parity calculation disclosed at col. 6, lines 36 to 42 of Steely, Jr. et al. Amended claim 12 now recites "merging the new data with the existing data so the new data replaces some existing data while other existing data remains," which is not disclosed by Steely, Jr. et al. or Grivna. As can be seen by the Examiner, this is not a parity calculation but a process to write an entire line of memory to a remote node with both new and old data when the new data is smaller than the entire line of memory. Accordingly, amended claim 12 is patentable over the combination of Steely, Jr. et al. and Grivna.

§ 103 Rejections of Claim 11

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Steely, Jr. et al. in view of Grivna and further in view of U.S. Patent No. 5,914,970 ("Gunsaulus et al."). The Examiner found that "Gunsaulus et al. teaches computing parity for a number of memory devices and writing the parity in one dedicated memory device." September 12, 2005 Final Office Action.

Amended claim 11 now recites "said writing a block of data from a local node to a remote node comprises computing parity over multiple blocks of data from a local memory of the local node and writing the parity to a remote memory of the remote node in a single operation," which is not disclosed by Gunsaulus et al., Grivna, or Steely, Jr. et al. As described in the Specification quoted below, Applicant believes that the prior art systems use two operations to send parity to a remote node.

> [I]f the same function was to be performed in previously developed system, parity of the local blocks must first be calculated and then saved in local memory. Next, the computed parity from local memory is transferred (as a DMA operation) to the remote node as a separate operation. With the communication for DMA engine write in accordance with an embodiment of the present invention, parity of the local blocks can be calculated (or computed) and transferred (as a DMA operation) to the remote node, thus saving an extra write operation to memory and an extra read operation from memory.

Specification, p. 13, lines 4 to 9. Accordingly, amended claim 11 is patentable over the combination of Steely, Jr. et al., Grivna, and Gunsaulus et al.

Claim Objection

The Examiner objected to claim 13 for a negative limitation. Applicant has amended claim 13 to remove the negative limitation and to add language that affirmatively defines the invention.

Claim Rejection under 35 U.S.C. § 112

The Examiner rejected claim 13 for failing to comply with the written description and enablement requirement of 35 U.S.C. § 112. Although Applicant respectfully disagrees with the Examiner, Applicant has amended claim 13 to expedite prosecution and to further clarify the language of the claimed invention. Amended claim 13 now recites "said writing a line of memory from a local node to a remote node comprises the writing the line of memory to a remote node using a same address offset of the line of memory at the local node," which is not disclosed or suggested by the cited references. Amended claim 13.

Amended claim 13 is supported and enabled by Table 4 on p. 26 of the Specification, which states, "[f]or memory copy writes, the ADDR field contains an offset from the base address of the sending node's send range, which is used as an offset from the base of the receiving node's receive

range for the respective communication link." Specification, p. 26, Table 4. Accordingly, Applicant requests the Examiner to withdraw the rejections of claim 13 under 35 U.S.C. 112.

In summary, claims 1 to 6 and 10 to 13 were pending in the present application. Applicant has amended claims 1 and 11 to 13, canceled claims 4 to 6. Applicant requests the Examiner to withdraw his claim objections/rejections and allow claims 1 to 3 and 10 to 13. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

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Respectfully submitted,

David C. Hsia
Attorney for Applicant(s)
Reg. No. 46,235